國立高雄海洋科技大學 100 學年度碩士班考試入學

微電子工程研究所—微電子學試題

(※須使用計算機)

1. Derive the closed-loop input resistance at the noniverting terminal of a noninverting amplifier, as shown in Fig.1. (20%)

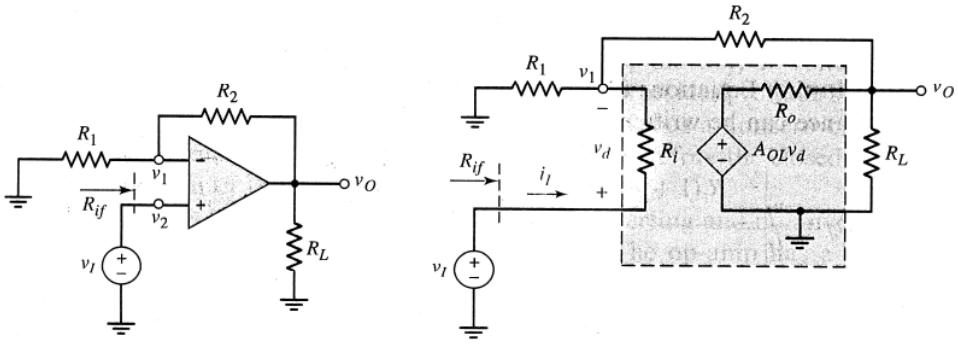

Fig.1

2. Determine the bias current effect in an op-amp circuit, (a) without bias current compensation, as shown in Fig. 2, and (b) with bias current compensation, as shown in Fig. 3. (R_1=10 kΩ, R_2=100 kΩ, I_{B1}=1.1 μA, I_{B2}=1.0 μA)(hint: R_3= R_1//R_2) (10%)

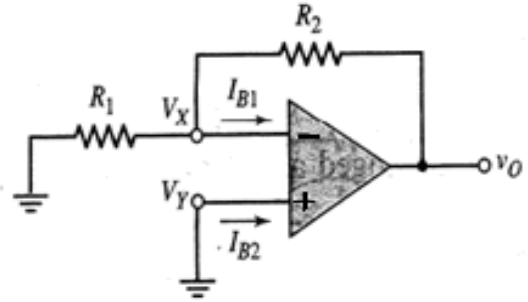

Fig.2

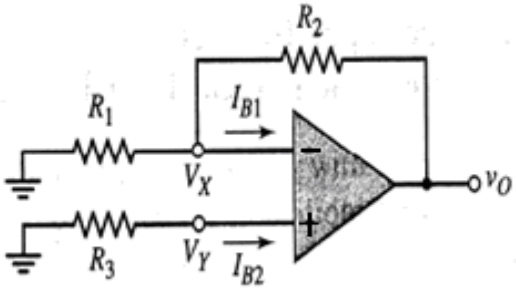

Fig.3

3. The Common-emitter circuit in Fig. 4 is biased at V_{cc}=20V. The maximum transistor power is $P_{D,max}$=20W and the current gain is β=80. (a) Determine R_L and R_B such that the maximum power is delivered to the load R_L. (b) find the value of V_p for the input signal that delivers the maximum power. (15%)

4. Figure 5 shows a basic two-transistor pnp current source. The transistor parameters are V_{EB}(on)=0.7V, β=40, and V_A=∞. Design the circuit such that I_o=0.25mA and determine the value of I_{REF}. (15%)

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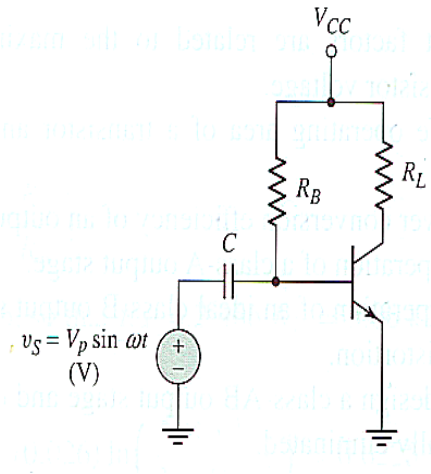

Fig. 4

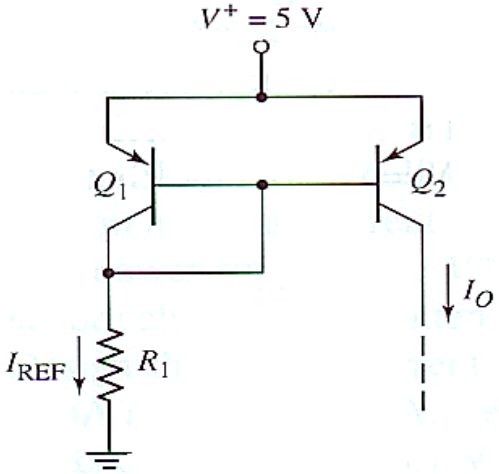

Fig. 5

5. 試解釋以下觀念:
   (a)請敘述 P 型半導體與 N 型半導體結合成 PN 二極體所形成內建電位的過程?爲何內建電位存在是必須的?
   (b)可否利用三用電錶(最小可測到 0.03V)來測試 PN 二極體的內建電位?並解釋之。
   (c) PN 二極體從順偏切換到逆偏(如圖 6 所示)則電流是否立即關閉?原因爲何? (20%)

6. The ac equivalent circuit if a CMOS common-gate circuit is shown in Fig. 7, The transistor parameters for M1 are : $V_{TN} = 0.5V$, $k_n` = 85\ \mu A/V^2$, $(W/L)_1 = 50$, $\lambda_1 = 0.05\ V^{-1}$, and for M2 and M3 are $V_{TP} = -0.5V$, $k_p` = 40\ \mu A/V^2$, $(W/L)_{2,3} = 50$, $\lambda_{2,3} = 0.075\ V^{-1}$. Determine the (a) small-signal parameter of the circuit (b) small-signal voltage gain and (c) input resistance R_i (d) output resistance R_O. (20%)

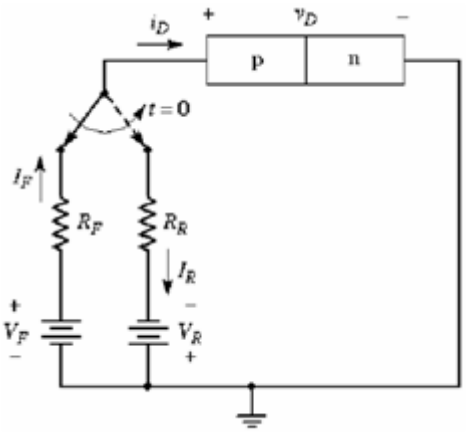

Fig. 6

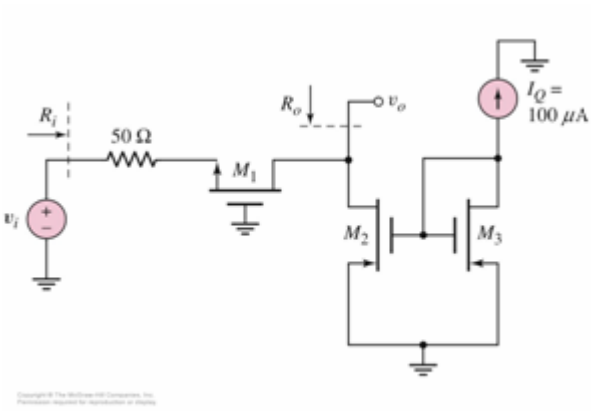

Fig. 7

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